IN THE SPECIFICATION:

Please replace the paragraphs beginning on page 4, line 11 to page 8, line 4, with the following:

According to an aspect of the present invention, there is provided a semiconductor device comprising: a memory cell array including a plurality of memory cells arranged in rows and columns, the memory cell array including a plurality of blocks in each one of which the memory cells are arranged; and a word-line select circuit including transfer transistors arranged in row and column directions, and configured to select at least one row of memory cells from the plurality of memory cells in a block, the word-line select circuit including: first transistors to which OV is to be applied; second transistors to which an intermediate level voltage is to be applied, the intermediate voltage being a voltage applied to a non-selected word line in a block selected in a writing operation; and third transistors to which a write voltage higher than the second voltage is to be applied, the third transistors being separated from the first transistors.

~~According to an aspect of the present invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of blocks, each of the blocks including memory cells arranged in rows and columns; a block select circuit configured to select one of the blocks of the memory cell array; a plurality of word-line-driving signal lines to receive voltages to be applied to a plurality of word lines in each block; and a plurality of transfer transistors having current paths thereof connected between the word-line-driving signal lines and the word lines of the each block, the transfer transistors being controlled by outputs from the block select circuit, any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, being separate from each other lengthwise and widthwise, one or more transfer transistors corresponding to another~~

~~word line or other word lines being interposed between the any two transfer transistors.~~

~~According to another aspect of the invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of blocks, each of the blocks including memory cells arranged in rows and columns; a block select circuit configured to select one of the blocks of the memory cell array; a plurality of word line driving signal lines to receive voltages to be applied to a plurality of word lines in each block; and a plurality of transfer transistors connected between the word line driving signal lines and the word lines of the memory cell array, the transfer transistors being controlled by outputs from the block select circuit, a first element isolation region, interposed between word line side terminals of some of the transfer transistors in the each block, having a narrower width than a second element isolation region, interposed between word line side terminals and word line driving signal line side terminals of other transfer transistors in the each block.~~

~~According to still another aspect of the invention, there is provided a semiconductor memory device comprising: a memory cell array including electrically programmable nonvolatile memory cells arranged in rows and columns; block select means for selecting one of blocks that are included in the memory cell array and each have a plurality of word lines; a plurality of word line driving signal lines to receive voltages to be applied to a plurality of word lines in each block; and a plurality of transfer transistors having current paths thereof connected between the word line driving signal lines and the word lines of the each block, the transfer transistors being controlled by outputs from the block select means, wherein any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or more transfer transistors corresponding to another word line or other word lines are interposed~~

~~between the any two transfer transistors.~~

~~According to still another aspect of the invention, there is provided a semiconductor memory device comprising: a memory cell array including electrically programmable nonvolatile memory cells arranged in rows and columns; block select means for selecting one of blocks that are included in the memory cell array and each have a plurality of word lines; a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and a plurality of transfer transistors connected between the word-line-driving-signal lines and the word lines of the memory cell array, the transfer transistors being controlled by outputs from the block select means, wherein a first element-isolation region, which is interposed between word-line-side terminals of some of the transfer transistors in the each block, has a narrower width than a second element-isolation region, which is interposed between word-line-side terminals and word-line driving-signal line-side terminals of other transfer transistors in the each block.~~

~~According to still another aspect of the invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of blocks, each of the blocks including electrically programmable nonvolatile memory cells arranged in rows and columns; a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and block select circuit configured to select one of blocks that are included in the memory cell array and each have a plurality of word lines, the block-select circuit includes a decoder section configured to decode row addresses assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster section configured to receive decode signals output from the decoder section, wherein any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or~~

~~more transfer transistors corresponding to another word line or other word lines are interposed between the any two transfer transistors~~.